CSP Manufacturing challenges and assembly reliability

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ABSTRACT

Although the expression of CSP is widely used by industry from suppliers to users, its implied definition had evolved as the technology has matured. There are "expert definition"- package that is up to 1.5 time die- or "interim definition". CSPs are miniature new packages that industry is starting to implement and there are many unresolved technical issues associated with their implementation. For example, in early 1997, packages with 1mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. Other changes included the use of flip chip die rather than wire bond in CSP. Nonetheless the emerging CSPs are competing with bare die assemblies and are becoming the package of choice for size reduction applications. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages.

The JPL-led MicrotypeBGA Consortium of enterprises representing government agencies and private companies have jointed together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. This talk will cover specifically the experience of our consortium on technology implementation challenges, including design and build of both standard and microvia boards, assembly of two types of test vehicles, and the most current environmental thermal cycling test results.

Bio:

Dr. Reza Ghaffarian has nearly 20 years of industrial and academic experience in mechanical, materials, and manufacturing process engineering. At JPL, Quality Assurance Office, he supports research and development activities in SMT, BGA, and CSP technologies for infusion into NASA's missions. He has authored over 50 technical papers and numerous patentable innovations. He received his M.S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 in engineering from University of California at Los Angeles (UCLA).